THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SHAY-PING T. WANG

Appeal No. 1997-3793
Application 08/294,235[1]

ON BRIEF

Before THOMAS, BARRETT, and BLANKENSHIP, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

[1] Application for patent filed August 22, 1994, entitled "Artificial Neuron And Method Of Using Same," which is a continuation of Application 08/076,602, filed June 14, 1993, now U.S. Patent 5,390,136, issued February 14, 1995.

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1-4 and 12-15. Claims 1, 3, 12, and 14 were amended (part of Paper No. 18) in response to a new ground of rejection in the Examiner's Answer and the new rejection was withdrawn (Supplemental Examiner's Answer, Paper No. 19).

We reverse.

BACKGROUND

The disclosed invention is directed to a neuron circuit and method of producing a neuron output which multiplies together a plurality of gated input signals x_i^{gi} and a predetermined weight, where at least one g_i is greater than one.

Claim 1, as amended by the amendment filed July 18, 1997, (part of Paper No. 18) is reproduced below.

1. A neuron circuit comprising:

> a multiplier circuit in communication with a plurality of gated input signals, each of said gated input signals representing one of a plurality of inputs to said neuron circuit raised to an exponential power of one of a plurality of gating functions g_i, said multiplier circuit for multiplying said gated input signals together to produce a product and for multiplying said product by

a predetermined weight to generate without a threshold comparison a neuron output signal;

wherein at least one of said plurality of gating functions g_i is greater than 1.

The Examiner relies on the following prior art:

Hata et al. (Hata), Gate Model Networks for Minimization of Multiple-Valued Logic Functions, Proceedings of the Twenty-Third International Symposium on Multiple-Valued Logic, IEEE, 24-27 May, 1993, pp. 29-34.

Claims 1-4 and 12-15 stand rejected under 35 U.S.C. § 102(a) as being clearly anticipated by Hata.

We refer to the Final Rejection (Paper No. 10) (pages referred to as "FR__") and the Examiner's Answer (Paper No. 17) (pages referred to as "EA__") for a statement of the Examiner's position and to the Appeal Brief (Paper No. 16) (pages referred to as "Br__") and the Reply Brief (Paper No. 18) (pages referred to as "RBr__") for a statement of Appellant's arguments thereagainst.

OPINION

The claims are grouped to stand or fall together. Claim 1 is taken as representative.

Appellant argues that Hata does not disclose an input signal raised to an exponential power of one of the gating functions g_i, wherein the gating function g_i is greater than 1. These limitations are found in all the independent claims.

The Examiner finds (FR2) that Hata discloses an input raised to a power at page 32, section 4, line 5 ("1. literal: x^s ..."), and equations (13) and (14). The Examiner further finds (EA7) that "x_1^2" at page 33, second column, line 14, shows x_1 raised to the power of 2.

Appellant responds that the notation in Hata, while using superscripts which could be easily confused with exponentiation, has nothing to do with exponentiation (Br3-5; RBr2-3).

Appellant is clearly correct. The term x_i^j is called a "literal" of input variable x, where a literal is a propositional variable or its negation. For an r-valued n-variable function F(X), $X=\{x_1,x_2,...,x_n\}$ is the set of n-variables, where x_i takes on values from $R=\{0,1,...,r-1\}$ (page 32, section 4). The term x_i^j refers to input variable x_i having the value j from the r values of set R, not x_i to the jth power. Since each input x_i can have one of r values, there are n·r inputs to each node in the hidden layer. Thus, in Example 3 on page 33, for a 2-variable ($X=\{x_1, x_2\}$) 4-valued ($R=\{0,1,2,3\}$) function there are 2·4=8 inputs ($x_1^0, x_1^1, x_1^2, x_1^3, x_2^0, x_2^1, x_2^2, x_2^3$). In the term x_1^2, x_1 refers to the first variable and the superscript 2 refers to the value 2, not a power. Because Hata does not disclose raising an input to a power greater than one, the anticipation rejection of claims 1-4 and 12-15 is reversed.

Although Appellant has elected to only argue the exponential power limitation, we also note that Hata does not disclose a multiplier circuit for multiplying the gated input signals together. In equation (13), the dots between the terms refer to a logical AND operation (page 30, right column, line 5), not a product. Figure 1 shows a summer as evidenced by equation (2). For this additional reason, the anticipation rejection of claims 1-4 and 12-15 is reversed.

<u>REVERSED</u>

JAMES D. THOMAS Administrative Patent Judge	)	
	)	
	)	BOARD OF PATENT
LEE E. BARRETT Administrative Patent Judge	)	APPEALS AND INTERFERENCES
	)	
HOWARD B. BLANKENSHIP Administrative Patent Judge	)	

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